Amendments to the Specification

Please replace the paragraph in the Specification page 19, lines 8-15 with the following amended paragraph:

The interposer 20A comprises an interposer base 21A, post electrodes 22A, rewiring layers 23, external connection terminals 24, a second insulation layer 26, etc. **As shown in FIG. 1, an upper principal surface 1, a lower principal surface 2, and a sidewall surface 3 connecting said upper principal surface 1 and said lower principal surface 2 define the interposer base 21A and are thus outer surfaces of the interposer base 21A.** The interposer base 21A is made of silicon. The post electrodes 22A are formed in the positions corresponding to the electrodes 13 of the semiconductor chip 11. **As shown in FIG. 1, each of the post electrodes 22A has a top end 6 exposed at the upper principal surface 1 of the interposer base and a bottom end 7 exposed at the lower principal surface 2 of the interposer base 21A.**

Please replace the paragraph in the Specification page 20, lines 20-26 with the following amended paragraph:

Directing attention first to the joining structure between the semiconductor chip 11 and the interposer base 21A, the semiconductor chip 11 is joined to the interposer base 21A without using adhesive or brazing materials, and without using joining processes utilizing heat such as welding. **As shown in FIG. 1, a top principal surface 5 of the semiconductor chip 11 is in direct contact with the lower principal surface 2 of the interposer base 21A.**

Please replace the paragraph in the Specification page 21, line 30 to page 22 line 5 with the following amended paragraph:

Moreover, as mentioned above, both the joint portion of the semiconductor chip 11 and the joint portion of the interposer base 21A have smooth surfaces. Therefore, in this embodiment, the semiconductor chip 11 and the interposer 20A

are integrated with each other by bringing the joint areas having smooth surfaces into contact with each other and pressing the joint areas against each other. **Thus, the top principal surface 5 of the semiconductor chip directly contacts the lower principal surface 2 of the interposer base 21A.**

Please replace the paragraph in the Specification page 24, line 26 to page 25 line 1 with the following amended paragraph:

The interposer base 21A is a piece that is cut out from a silicon wafer. **The interposer base 21A is defined by an upper principal surface 1, a lower principal surface 2, and a sidewall surface connecting the upper principal surface 1 to the lower principal surface 2.** The through holes 31A are formed in positions in the interposer base 21A corresponding to the electrodes 13 of the semiconductor chip 11. **As shown in FIG. 2A, the through holes extend between the upper and lower principal surfaces 1 and 2 of the interposer base 21A.** The cross section of each through hole 31A is larger than the area of each electrode 13. An SiO.sub.2 film (not shown) as a protective film is formed on the entire surface of the interposer base 21A.

Please replace the paragraph in the Specification page 25, lines 12-25 with the following amended paragraph:

The semiconductor chip 11 and the interposer base 21A configured as described above are put inside a vacuum unit. The through holes 31A and the electrodes 13 are positioned. Then, with reference to FIG. 2B, the smooth surfaces (mirror surfaces) of the semiconductor chip 11 and the interposer base 21A are brought into contact with and pressed against each other. The smooth surfaces are thus put in tight contact with each other to be integrated with each other without using adhesive or the like. As a result, the semiconductor chip 11 and the interposer base 21A are firmly joined together (joining process) **with the top principal surface 5 of the semiconductor chip 11 being in direct contact with the lower principal surface of the interposer base 21A**.

Please replace the paragraph in the Specification page 26, lines 15-25 with the following amended paragraph:

Then, copper plating is applied to the inside of the electrode holes 34 so as to form the post electrodes 22A inside the electrode holes 34 as shown in FIG. 3C. **The post electrodes 22a have a top end 6 exposed at the upper principal surface 1 and a bottom end 7 exposed at the bottom principal surface 2.** Since the post electrodes 22A are formed by depositing copper directly on the barrier metal portions 14, the post electrodes 22A are formed directly on the barrier metal portions 14 (i.e. electrodes 13). It is to be noted that the post electrodes 22A can be formed by either electrolytic plating or nonelectrolytic plating.

Please replace the paragraph in the Specification page 27, lines 3-14 with the following amended paragraph:

After the second resist 35 is formed, copper plating is applied to the inside of the openings 36. Thus, as shown in FIG. 4B, the rewiring layers 23 are formed inside the openings 36. Since the rewiring layers 23 are formed directly on the upper ends **(i.e., top ends 6)** of the post electrodes 22A, good electrical connections are established between the post electrodes 22A and the rewiring layers 23. It is to be noted that the rewiring layers 23 can also be formed by either electrolytic plating or nonelectrolytic plating.

Please replace the paragraph in the Specification page 31, lines 12-24 with the following amended paragraph:

The smooth surfaces are thus put in tight contact with each other as shown in FIG. 6B and integrated with each other without using adhesive or the like. As a result, the semiconductor chip 11 and the interposer base 21A are securely joined together**, and the lower principal surface 2 of the interposer base 21A is in direct contact with the top principal surface 5 of the semiconductor chip 11**. As can be seen, even if the surfaces of the semiconductor chip 11 and the interposer base 21A are covered with the

corresponding PI films (resin films) 16 and 28, the semiconductor chip 11 and the interposer base 21A can be joined together without using adhesive or the like by just being brought into contact with and pressed against each other.

Please replace the paragraph in the Specification page 33, lines 15-29 with the following amended paragraph:

After the post electrode forming process is completed, the integrating process is performed. In the integrating process, the semiconductor chip 11 and the interposer base 21S are placed in a vacuum unit, and smooth surfaces (mirror surfaces) of the semiconductor chip 11 and the interposer base 21A are brought into contact with and pressed against each other in a predetermined vacuum environment. The smooth surfaces are thus put in tight contact with each other and integrated with each other without using adhesive or the like. As a result, as shown in FIG. 8B, the semiconductor chip 11 and the interposer base 21A are securely joined together**, and the lower principal surface 2 of the interposer base 21A is in direct contact with the top principal surface 5 of the semiconductor chip 11**.

Please replace the paragraph in the Specification page 35, line 32 to page 36, line 10 with the following amended paragraph:

The semiconductor device 10D of this embodiment is characterized in that plural post electrodes 22A (only two post electrodes 22A are shown in FIG. 9) are disposed in one through hole 31B. As shown in FIG. 10A, the through hole 31B formed in an interposer base 21B has a greater area than the area of the through hole 31A in the first-third embodiments. In the integrating process, as shown in FIG. 10B, the portion of the interposer base 21B around the through hole 31B is directly joined to the semiconductor chip 11**, so that the lower principal surface 2 of the interposer base 21B is in direct contact with the top principal surface 5 of the semiconductor chip 11**.

Please replace the paragraph in the Specification page 37, line 32 to page 38,

line 8 with the following amended paragraph:

The smooth surfaces are thus put in tight contact with each other and integrated with each other without using adhesive or the like. As a result, as shown in FIG. 12B, the semiconductor chip 11 and the interposer base 21B are securely joined together**, so that the lower principal surface 2 of the interposer base 21B is in direct contact with the top principal surface 5 of the semiconductor chip 11**. In this joining state, a gap is formed between the outer circumferential surface of the protective layer 17 and the inner circumferential surface of the through hole 31B as shown in FIG. 12B.

Please replace the paragraph in the Specification page 41, lines 18-25 with the following amended paragraph:

The semiconductor chips 11 are joined at back faces 11a thereof to the corresponding cavities 40A, so that the semiconductor chips 11 are secured to the interposer base 21F. As in the case of the above-described embodiments, the small base surface joining method is used for joining the semiconductor chips 11 and the interposer base 21F together **so that the lower principal surface 2 of the interposer base 21F is in direct contact with the top principal surface 5 of the semiconductor chip 11**.

Please replace the paragraph in the Specification page 42, lines 23-33 with the following amended paragraph:

The semiconductor device 10J of the tenth embodiment shown in FIG. 18 is characterized in that a cavity 40B formed in the interposer base 21G from the lower surface thereof and that openings 43 are formed in predetermined portions of a top plate section 42 facing the semiconductor chips 11. In this embodiment, the top plate section 42 around the openings 43 are surface joined to back faces 11a of the semiconductor chips 11 by small base surface joining **so that the lower principal surface 2 of the interposer base 21G is in direct contact with the top principal surface 5 of the semiconductor chip 11**.

Please replace the paragraph in the Specification page 44, lines 13-26 with the following amended paragraph:

The semiconductor device 10L of the twelfth embodiment shown in FIG. 20 is configured such that plural cavities 40C are formed in the interposer base 21H from the upper surface thereof, and a through hole 31D is formed in a bottom plate section 45 of each cavity 40C. An insulation film 15 of the semiconductor chip 11 is joined to the bottom plate section 45 around the through hole 31D by small base surface joining, and thus secured to the interposer base 21H. **Thus, in this embodiment the upper surface of interposer base 21H corresponds to the lower principal surface 2 and the surface of the semiconductor chip 11 on which the electrodes 13 are formed in the semiconductor chip's top principal surface 5. Accordingly, the lower principal surface 2 of the interposer base 21G is in direct contact with the top principal surface 5 of the semiconductor chip 11.** Post electrodes 22A are configured to extend through the corresponding through holes 31D to the lower surface side of the interposer base 21H.

Please replace the paragraph in the Specification page 53, line 28 to page 54, line 5 with the following amended paragraph:

As in the above-described embodiments, the light emitting element 55 and the light receiving element 56 are pressed against the interposer base 21M in a vacuum environment, so that the smooth surfaces are put in tight contact with each other**, and the lower principal surface 2 of the interposer base 21M is in direct contact with the top principal surfaces 5 of the light emitting element 55 and the light receiving element 56**. As a result, the light emitting element 55 and the light receiving element 56 are integrated with and firmly joined to the interposer base 21M without using adhesive or the like (small base surface joining method).